MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

Sponsored by CMR Educational Society

(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2008 Certified)

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MASTER OF TECHNOLOGY
VLSI & EMBEDDED SYSTEMS

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE COVERAGE SUMMARY AND QUESTION BANK
ACADEMIC YEAR: 2016-2017

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
M.TECH – VLSI & EMBEDDED SYSTEMS
COURSE STRUCTURE

I YEAR I SEMESTER

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R15D6801	VLSI Technology & Design	4	-	3	25	75
2	R15D6802	CPLD & FPGA Architectures & Applications	4	-	3	25	75
3	R15D6803	Embedded System design	4	-	3	25	75
4	R15D6804 R15D6805 R15D6806	ELECTIVE-I 1.Digital System Design 2.CMOS Analog Integrated Circuit Design 3.Hardware Software Co-design	4	-	3	25	75
5	R15D6807 R15D6808 R15D6809	ELECTIVE-II 1.CMOS Digital Integrated Circuit design 2.Algorithms for VLSI Design Automation 3.Advanced Digital Signal Processing	4	-	3	25	75
6	R15D5802 R15D5803 R15D5812	OPEN ELECTIVE –I 1.Advanced Operating Systems 2.Computer System Design 3.Web Services and Service oriented Architecture	4	-	3	25	75
7	R15D6881	VLSI Laboratory	-	3	2	25	75
8	R15D6882	Technical Seminar-I	-	-	2	50	-
Total			24	3	22	225	525

I YEAR II SEMESTER

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	R15D6810	Embedded Real Time Operating Systems	4	-	3	25	75
2	R15D6811	CMOS Mixed Signal Circuit Design	4	-	3	25	75
3	R15D6812	Low Power VLSI Design	4	-	3	25	75
4	R15D6813 R15D6814 R15D6815	ELECTIVE – III 1.Adhoc –Wireless Networks 2.Digital Signal Processors & Architectures 3.Embedded Networking	4	-	3	25	75
5	R15D6816 R15D6817 R15D6818	ELECTIVE- IV 1.System On Chip Architecture 2.Design For Testability 3.Multimedia Signal Coding	4	-	3	25	75
6	R15D5805 R15D5810 R15D5816	OPEN ELECTIVE- II 1.Natural Language Processing 2.Advanced Network Programming 3.Grid and Cloud Computing	4	-	3	25	75
7	R15D6883	Embedded Systems Laboratory	-	3	2	25	75
8	R15D6884	Technical Seminar-II	-	-	2	50	-
Total			24	3	22	225	525

II YEAR I SEMESTER

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	-	Project Review Seminars	-	-	4	-	-
2	-	Project Work	-	-	18	-	-
Total			-	-	22	-	-

II YEAR II SEMESTER

S.NO.	SUBJECT CODE	SUBJECT	L	T/P/D	C	MAX MARKS	
						INT	EXT
1	-	Project Work	-	-	22	-	-
2	-	Project Viva-voce	-	-	-	-	-
Total			-	-	22	-	-

I-SEMESTER

CONTENTS

VLSI TECHNOLOGY AND DESIGN

UNIT –I: Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds} – V_{ds} relationships, Threshold Voltage V T , G m , G ds and ω o , Pass ransistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu} /Z_{pd} , MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II: Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III: Combinational Logic Networks:

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks,Gate and Network testing.

UNIT –IV: Sequential Systems:

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V: Floor Planning:

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005,PHI.

2. Modern VLSI Design – Wayne Wolf, 3 rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC

Press, 2011.

2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2 nd Ed., Addison Wesley.

VLSI TECHNOLOGY AND DESIGN

COURSE COVERAGE SUMMARY

S.No	TEXT BOOK TITLE	Chapters in Text Book	Units / Topics Covered	AUTHOR	PUBLISHERS	EDITION
1	Essentials of VLSI Circuits & Systems	1,2	Unit I-Review of Microelectronics and Introduction to MOS Technologies	K.Eshraghian D,A.Pucknell	PHI	2005
2	Modern VLSI Design	2,3	Unit II-Layout Design and Tools,Logic Gates and Layouts	Wayne Wolf	Pearson	3rd ed., 1997
		4	Unit III-Combinational Logic Networks			
		5	Unit IV-Sequential Systems			
		7,8	Unit V-Floor Planning			

Code No: C0601, C5503, C7703, C6803, C5703, C7003, C4507, C3803 JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH I SEMESTER EXAMINATIONS, APRIL/MAY-2012

VLSI TECHNOLOGY AND DESIGN

Time: 3hours Max. Marks: 60 Answer any five questions

All questions carry equal marks

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1. Draw the circuits for n-MOS, p-MOS and C-MOS Inverter and explain about their operation and compare them.

2.a) Explain about scalable Design rules related to NMOS and CMOS Technologies.
b) What are the issues involved in driving large capacitive loads in VLSI circuits? Explain.

3. Explain the following
a) Why is n-diffusion to p-diffusion spacing is so large?
b) Why metal - metal spacing is larger than ploy-ploy spacing?
c) What are the effects of scaling of V_t?

4.a) Explain how to reduce the cross talk by using ground wire to minimize cross talk.
b) Explain how fan-out and path delay influences delay in combinational networks.

5.a) What are various floor planning methods? Discuss in brief.
b) Explain the delay in combinational logic network and how combinational delay can be reduced.

6.a) What are the various issues in system-on-chip design? Explain it briefly.
b) Develop a sequence of tests for the '01' string recognizer which tests every combinational gate for both stuck -at -0 and stuck -at-1 faults.

7.a) Explain how the extracting a data path and controller from the ASM chart.
b) Explain how would you translate a register transfer structure into a legal two phase latched sequential machine give an example.

8.a) Explain the sequential testing for testing a sequential machine and time-frame expansion of a sequential test.
b) Write short notes on Chip design methodologies.

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Code No: C3803, C0601, C7003, C5503, C7703, C4507, C6803, C5703

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, March-2011

VLSI TECHNOLOGY AND DESIGN

Time: 3hours Max. Marks: 60 Answer any five questions

All questions carry equal marks

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1. a) What is latch-up condition in CMOS circuits? How it can be eliminated.
   b) What are the deficiencies of MOS technology? How do we over come them? [12]

2 a) explain the scalable design rules with equation
b) Explain the pseudo-NMOS logic during the low to high transition. [12]

3 a) Explain the delay in combinational logic network and how combinational delay can be reduced.
b) What are various switch logic circuits? Compare their merits and demerits. [12]

4. Explain about 1 -φ clocking rules for flip-flops and 2 -φ clocking disciplines for latches. [12]

5. a) What are various floor planning methods? Explain them clearly.
b) With relevant diagrams explain about various Floor planning methods used in Layout design. [12]

6) a) Explain the technology independent and technology dependant strategies of logic optimization used in logic synthesis
a) Explain briefly how the hardware/software Co-simulation and co- synthesis issued are addressed. [12]

7 a) Briefly explain the design validations in the floor planning.
b) Describe the Placement and routing in floor planning. [12]

8.Write short notes of the following:
a) power optimization.
b) Inductive interconnect delays. [12]

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech I Semester Examinations, April/MAY-2012
VLSI TECHNOLOGY AND DESIGN
(COMMON TO EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)
Time: 3hours Max. Marks: 60

Answer any five questions
All questions carry equal marks

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1. Design BiCMOS inverter with neat sketches and explain.

2. Explain Latch –up problem in CMOS circuits and discuss reducing methods.

3. Design a CMOS layout circuit for the function Y=((A+B).C.)'?

4. Calculate K,H,50% delay of the Buffers required when a minimum size inverter drives a metal 1 Wire that is 200 λ ∗3 λ in this case ,Ro=4.9kΩ and Co=0.69fF while Rint=5.34Ω and cint=15fF+90.1fF=105.1fF.

5. Explain in detail about logic & Inter connect Designs with examples.

6. Explain LSSD with Latch example.

7.a) How ASAP & ALAP schedules are differ with data flow graph?
b) Write any one of architectural method for reducing power consumption.

8. Explain a simple Dog Leg routing algorithm.

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Code No: D109115503

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Regular Examinations March 2010

VLSI TECHNOLOGY AND DESIGN

(Common to Embedded Systems, Digital Systems & Computer Electronics, Digital Electronics & Communication Systems, VLSI System Design / VLSI / VLSI Design, Embedded Systems & VLSI Design, VLSI& Embedded Systems, Electronics & Communication Engineering, Systems & Signal Processing)

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

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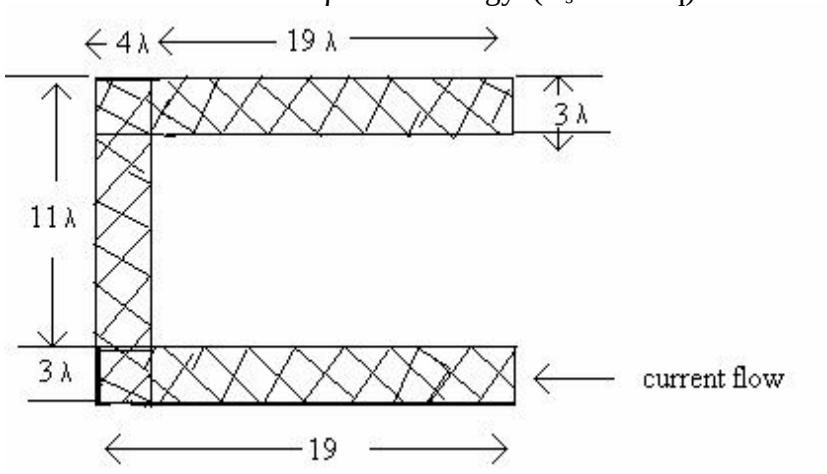
1. a) Explain the fabrication procedure for P-Well CMOS technology.
   b) What are the differences between CMOS and BiCMOS technologies in fabrication?

2. a) Explain how to estimate propagation delay?
   b) Calculate the resistance of the polysilicon wire shown in figure. This polysilicon wire is to be fabricated with a 1µm technology. (R_s = 4Ω/sq).

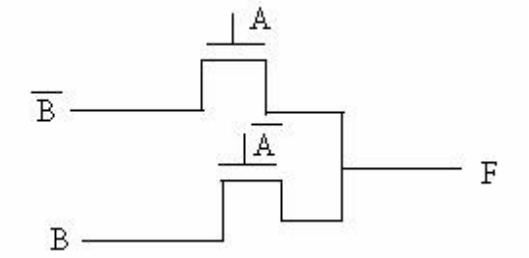


   c) Determine Z_{pu} /Z_{pd} for NMOS inverter driven by another inverter.

3. a) Design a symbolic layout for a complementary CMOS circuit that implements $F= \overline{A + BC}$.
   b) What are the various properties of transmission gate logic?

4. a) What are various limitations of scaling?
   b) What is via? Why these are required in circuit design.

5. Consider the circuit shown in figure.
   i) Determine the logic function F.
   ii) Design a circuit to implement the same logic function using NOR gates.
   iii) Draw a transistor level schematic and use CMOS technology.



6. a) What is clock skew? How it is calculated?
   b) Explain how to optimize power for sequential circuits?

7. Explain Floor-Planning methods for a chip in detail.

8. Write short notes on
   a) Resistive and inductive interconnect delay.
   b) High level Synthesis.

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I SEMESTER EXAMINATIONS, APRIL/MAY-2013
VLSI TECHNOLOGY AND DESIGN

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

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1.a) Explain the various steps of CMOS fabrication with neat diagrams.
b) Compare the CMOS and BiCMOS technologies.

2. Explain the following terms:

a) g_m b) G_{ds} c) V_t d) w_0

3.a) What are different layout design rules? Explain them with suitable examples.
b) What is wires and vias? How to design them.

4.a) Design a NOR gate using pass transistor logic.
b) Derive the propagation delay τ_{PHL} for inverter.

5.a) What are the different simulations available to test a combinational circuits? Explain them.

b) Draw the layout for CMOS NAND gate.

6.a) Draw the circuit diagram of six transistor SRAM cell and explain its working.
b) How power in sequential circuits is optimized? Explain any two such methods.

7.a) What is Floor Planning? Explain it with examples.
b) Explain the architecture for low power VLSI design.

8. Write short notes on the following:
a) High level synthesis
b) Latch up.

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-I:

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic
Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex
Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD
Implementation of a Parallel Adder with Accumulation.

UNIT-II:

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures,
Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 andXC4000 Architectures.

UNIT -IV:

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and
ACT3 Architectures.

UNIT -V:

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International
Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design.

COURSE COVERAGE SUMMARY FOR CPLD & FPGA ARCHITECTURE

S.No	TEXT BOOK TITLE	Chapters in Text Book	Units / Topics Covered	AUTHOR	PUBLISHER	EDITION
1	Digital System Design	2,3	Unit I-Introduction to Programmable Logic Devices	charles H.Roth jr,Lizy Kurian john	cengage learning	--
2	Field Programmable GateArray Technology	1	Unit II-Field Programmable Gate Arrays	Stephen M.Trimberger	Springer International	
		2	Unit III-SRAM Programmable FPGAs			
		4	Unit IV-Anti Fuse Programmed FPGAs			
		3	Unit V-Design Applications			

Code No: A5706

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH I SEMESTER EXAMINATIONS, APRIL/MAY-2012 CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

(VLSI SYSTEM DESIGN)

Time: 3hours Max.Marks:60 Answer any five questions

All questions carry equal marks

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1.a) Distinguish between ALTERA's CPLD and CYPRESS Flash 370 device.
b) Compare the AMD's CPLD match 1 to 5.

2.a) Show the PLA implementation of a Binary adder of 4 bit.
b) Explain about the ALTERA's third generation architecture of MAX7000 family with neat diagram.

3.a) Explain about the alternative realization for state machine using micro programming.
b) Explain about the top-down design approach of state machine with an example.

4.a) Explain about one hot state machine with state table and state diagrams.
b) Develop one hot state diagram for a sequence checker whose output is '1' whenever the sequence 0101 is detected. Also specify its Transition Table.

5.a) Explain the extended petrinets for parallel controllers
b) Explain about linked state machine for a dice game.

6.a) Explain about the datapath and functional partition of FSM system level design
b) Design a binary multiplier control using one-hot method.

7. Explain the complete design flow to implement a 4 bit Ripple-carry adder circuit on to FPGA using an EDA tool. Also explain the timing simulation for the same.

8. Write a brief note on any two:
a) Floor plan
b) Optimized reconfigurable cell array.
c) Speed performance of different CPLDs.

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Code No: C6106, C0608, C7702, C6802, C5702, C6506

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY

HYDERABAD M.TECH I SEMESTER EXAMINATIONS

APRIL/MAY-2012

CPLD & FPGA ARCHITECTURES AND APPLICATIONS

Time: 3hours Max.Marks:60 Answer any five questions

All questions carry equal marks

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1.a) Explain the PLA design for the fallowing

f=x'y'z+x'yz+xyz+xy'z' .

b) Explain speed performance and system programming.

2. Consider any logic block and explain routing architecture.

3. Explain the design flow technology mapping for FPGA's.

4. Explain state machine chart using micro programming linked state machine.

5. Explain hot state machine with an example.

6. Explain the front end and dsign tools for FPGA.

7. Explain the design flow using FPGA's.

8. Write short notes on the following

i) Design of parallel adder cell.

ii) Sequential circuit.

iii) Parallel controllers.

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Code No: C6106, C0608, C7702, C6802, C5702, C6506

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations March/April-2011

CPLD & FPGA ARCHITECTURES AND APPLICATIONS

(COMMON TO COMMUNICATION SYSTEMS, DIGITAL SYSTEMS & COMPUTER ELECTRONICS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI&EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN, WIRELESS & MOBILE COMMUNICATIONS)

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

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1. a. Explain the design of altera flex logic -1000 series cpld.
   b. Explain The Pla Design With An Example. [12]

2. Explain Cypres Flash 370 Device Technology. [12]

3. a. Explain the fpga with channel and channel less gate array. Explain routing technique implemented.
   b. Explain the design aspects of altera's flex 8000 fpga. [12]

4. Explain the microprograming linked state machine with an example. [12]

5. a. Explain the properties of petrinets.
   b. Explain the state machine for petrinets with an example. [12]

6. Explain the design flow using fpga mentor graphics eda tool. [12]

7. Design a parallel adder sequential circuit. [12]

8. Write short notes on the following.
   i. Speed performance of actel.
   ii. Speed performance in system programmability.
   iii. Asic design flow. [12]

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Code No: D109110608

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Regular Examinations March/April 2010

CPLD& FPGA ARCHITECTURES AND APPLICATIONS

(COMMON TO DSCE, WIRELESS & MOBILE COMMUNICATION, VLSI SYSTEM DESIGN/VLSI/VLSI DESIGN, COMMUNICATION SYSTEMS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS)

Time: 3hours Max.Marks:60 Answer any five questions

All questions carry equal marks

- - -

1. (a). Draw and explain architecture of PLD.

   (b). With diagram explain Functional block.

2. (a). Explain Architecture of Altera MAX 5000 series CPLD.

   (b). Explain the ACT 2 and ACT 3 Logic Modules.

3. (a). Draw and explain the General Block diagram of FPGA.

   (b). Discuss Speed performance of different FPGAs.

4. (a). Write short note on extended Petri nets for parallel controllers.

   (b). Explain about One Hot State machine.

5. (a). Explain Basic concepts of Petri nets for state machines.

   (b). Explain briefly about Front end Design tools for ASICs.

6. Explain in detail about Design flow using FPGAs.

7. (a). Explain about Parallel Adder Cell.

   (b). Briefly explain about Serial Multiplier with Parallel Addition.

8. Write short notes on any TWO of the following:

   (i). EDA tools

   (ii).Speed performance of different

   CPLDs. (iii).Applications of CPLDs

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Code No: A5706 NR

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Regular Examinations March 2010
CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(VLSI SYSTEM DESIGN)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks
- - -

1.a) Compare Altera FLEX Logic-10000 series CPLD with Cypres FLASH 370 device technology.
b) What are complex programmable logic devices? Briefly outline salient features of these devices and applications.

2.a) How many macrocells available in these CPLDs:
i) EPM 7032
ii) EPM 7064
iii) EPM 7128S
iv) EPM7160S.
b) Briefly state the difference between CPLPs having sum-of-products architecture and look up table architecture.

3.a) State the possible preset configurations of a MAX7000s.
b) What can be done with the macrocells in LAB that are not connected to I/O pins?
c) Draw a neat block schematic of a logic element of FLEX10000.

4.a) Give examples of fuse link in an array logic for a CPLD.
b) What are the possible structures of the CLBs? Draw the structures.

5.a) Compare the ACTEL's Act-1,2,3 performance.
b) Design a 4 bit Ripple counter using one-hot state machine.

6. Design a digital system which performs a binary multiplication using Asm chart and design the controller of their system. Implement the same using PLA.

7. Explain the complete design flow to implement a Ripple-carry adder circuit on to FPGA using an EDA tool. Also explain the timing simulation for the same.

8. Write a brief note on:
a) Floor plan
b) Mentor graphic EDA tool "FPGA Advantage".

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MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

UNIT –I:ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store

Instructions,PSR Instructions, Conditional Instructions.

UNIT –III:ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic,Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

3. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

COURSE COVERAGE SUMMARY

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

S.No	TEXT BOOK TITLE	Chapters in Text Book	Units / Topics Covered	AUTHOR	PUBLISHER	EDITION
1	ARM Systems Developers Guides- Design & Optimizing System Software	1,2	I-ARM Architecture	Andrew N. Sloss, Dominic Symes, Chris Wright,	Elsevier	2008
		3	Unit II- ARM Programming Model-I			
		4	Unit III- ARM Programming Model-II			
		5,6	Unit IV- ARM Programming			
		12	Unit-Memory Management			

Code No: C3806, C0604, C7006, C5501, C7701, C5701, C6801

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH I - SEMESTER EXAMINATIONS, APRIL/MAY-2012

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

(COMMON TO VLSI SYSTEM DESIGN, VLSI & EMBEDDED SYSTEMS)

Time: 3hours Max. Marks: 60 Answer any five questions

All questions carry equal marks

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1.a) Explain the hardware units and devices in an Embedded system.

b) Give the classification of embedded systems.

2.a) Discuss in detail the architecture of 8051 microcontroller.

b) Explain the need for counters.

3. Discuss in detail memory and I/O devices interfacing to the microcontroller.

4.a) Compare Continuous timer blocks and Switched capacitor blocks.

b) Draw the architecture of Programmable system-on-chip.

5.a) Explain in detail the architecture of Embedded RISC processor.

b) Explain the modes of operation of ARM processor.

6.a) Explain the following terms:

i) Context switch
ii) Interrupt latency

b) Explain the device drivers for internal programmable timing devices.

7. Describe the following:

a) Serial communication protocols b) SDMA

8. Write notes on the following: a) Embedded software
b) I/O ports

c) Digital blocks.

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Code No: C3806, C0604, C7006, C5501, C7701, C5701

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I - Semester Examinations, October/November-2011

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

(COMMON TO DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS, DIGITAL SYSTEMS & COMPUTER ELECTRONICS, ELECTRONICS & COMMUNICATION ENGINEERING, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI SYSTEM DESIGN)

Time: 3hours Max. Marks: 60 Answer any five questions

All questions carry equal marks

1 a. What is an Embedded system? How is it different from a personal computer? 4M

b. Explain the steps involved in the design process of an embedded system. 8M

2. a. Explain how External memory is interfaced to 8051. 8M

b. Discuss the need for Timers. 4M

3. a. Write notes on the various Memory arbitration schemes. 6M

b. Explain about PIC controllers. 6M

4. a. Discuss in detail PSOC architectures. 8M

b. Explain about Digital blocks. 4M

5. Explain the Register set and instructions of ARM processor. 12M

. a. What is context switch? When does it take place? 4M

b. Explain in detail serial port device driver. 8M

7. a. Explain in detail the Ethernet protocol. 6M

b. Discuss about the External bus interface. 6M

8. Write short notes on the following:

i. Formalization of system design 4M

ii. PIC Controllers 4M

Interrupt latency. 4M

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I - Semester Examinations, March/April-2011

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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1.a) What are the issues in designing embedded system?

b) Why does a processor system always need an interrupt handle? [6+6]

2.a) Explain the need of a watchdog times and reset after the watched time.

b) What are the advantages of an ASIP for design of an embedded system? [6+6]

3. Explain the serial communications control operation in 8051 in different modes of operation. [12]

4.a) Draw a neat program model of ARM and explain its different modes of usage.

b) Explain the multiple register transfer instruction set of ARM processor. [6+6]

5.a) Explain events management? How are inter-task communication objects used for communication and synchronization?

b) How do we choose scheduling strategy for the periodic, a periodic and sporadic tasks? [6+6]

6.a) How do you create a counsiling semaphore?

b) How do we initiate round robin time series scheduling?

c) How do you let a lower priority task executes in a preemptive scheduler? [6+6]

7.a) Discuss about I2C bus communication with its devices.

b) How does CAN differ from I2C? [6+6]

8. Write brief note on:

a) SDMA

b) Continuous timer blocks in PSOC. [12]

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY
HYDERABAD M.Tech I SEMESTER EXAMINATIONS,
APRIL/MAY-2013

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

(EMBEDDED SYSTEMS)

Time: 3hours **Max.Marks:60**

Answer any five questions. All questions carry equal marks

1.a) Explain different Hardware units in Embedded systems.

b) Explain the design process for an embedded application.

c) Explain how embedded systems are classified.

2.a) Explain the memory mapped I/O and I/O mapped I/O.

b) Explain how 8051 is interfaced to external memory.

c) What are the different timers in 8051 and its modes?

3.a) Explain the ARM processor architecture.

b) Give overview of programmable system on chip (PSOC).

4.a) Explain context switching with an example. What is Pre-emptive scheduling?

b) Explain the procedure to write a device driver using interrupt service routine.

5. Explain serial communication protocols with an example.

6. A)What is the difference between RISC and CISC Architecture?

b) Explain continuous timer blocks and switched capacitor blocks.

7. Explain PIC ontrollers.

8. Write short notes on the following:

a) Ethernet protocol.

b) ARM6TDMI based embedded system.

DIGITAL SYSTEM DESIGN

(ELECTIVE -I)

UNIT -I:Minimization and Transformation of Sequential Machines:

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine

minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II:Digital Design:

Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:SM Charts:

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:Fault Modeling & Test Pattern Generation:

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault

dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques,Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:Fault Diagnosis in Sequential Circuits:

Circuit Test Approach, Transition Check Approach – State identification and fault detection

experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5 th Ed., Cengage Learning.

2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A.

Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2 nd Ed., 2001, TMH

2. Digital Design – Morris Mano, M.D.Ciletti, 4 th Edition, PHI.

3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

DIGITAL SYSTEM DESIGN

COURSE COVERAGE SUMMARY

S.No	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR(S)	PUBLISHERS	EDITION
1	Fundamentals of Logic Design	I,II	Charles H. Roth	Cengage Learning	5 th Ed.
2	Digital Systems Testing and Testable Design	IV	Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman	John Wiley & Sons Inc.	
3	. Logic Design Theory	III,IV	N. N. Biswas	PHI	
4	. Switching and Finite Automata Theory	V	Z. Kohavi	TMH	2 nd Ed., 2001

Code No: 5106B **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, February - 2014

DIGITAL SYSTEM DESIGN

(Digital System and Computer Electronics)

Time: 3 Hours **Max. Marks: 60**

Instructions:

i) Part A is compulsory Question for 20 marks.
ii) Part B consists of five questions with "either" "or" pattern. The student has to answer any one. However students have to answer five questions from Part B (numbered from 2 to 6)

PART - A (Answer all sub questions)

5 × 4 marks = 20

1.a) Define Race, also explain the terms critical race and non critical race.

b) Implement a full adder using PAL

c) Draw and explain different components of an SM chart.

d) Draw the circuit which realizes the function $f(x) = x_1x_2 + x_3 x_4$ using AND- OR gates using Boolean difference method obtain the test set to detect SA0 fault on input line x_1 of the circuit.

e)Write the rules to construct a distinguishing sequence of a machine

PART – B **5 × 8 marks = 40**

Answer either "a" or "b" from each question

2.a) Define flow table . Obtain flow table for a sequential circuit with two inputs x_1 and x_2 and one output z for the following data. The initial input state is $x_1 = x_2 = 0$. The output value is to be 1 if and only if the input state is $x_1 = x_2 = 1$ and the preceding input state is $x_1 = 0$, $x_2 = 1$.

OR

b) Classify hazards and implement the following Boolean function by a hazard free OR-AND network $f=\sum(0,2,6,7)$.

3.a) Realize a 4-bit BCD to gray code converter using PLA.

OR

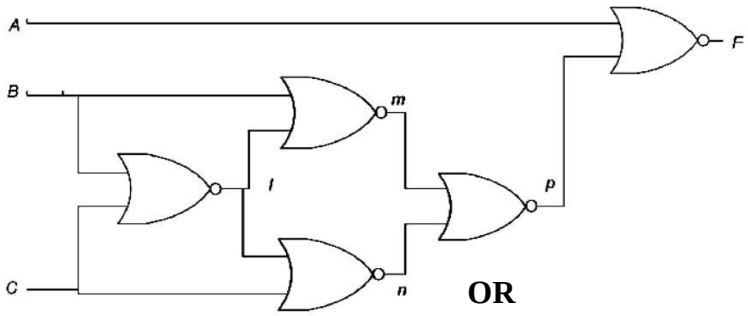
b) Draw the block diagram of a parallel binary divider and obtain the state graph for divider control circuit.

4.a) Derive the state machine chart for a binary multiplier and realize using a PLA.

OR

b)Derive the state machine chart for a dice controller.

5.a) Apply PODEM algorithm to derive a test to detect a *l* s-a-1 fault for the combinational circuit shown below.



OR

b) Explain signature analysis technique using an example.

6.a) Explain fault detection in a sequential circuit using circuit test approach with an example.

OR

c) i) What is a homing sequence? Write the rules to construct a homing sequence of machine.

ii) Conduct a homing experiment and determine final state of the given machine

Machine M_1

Present State	Next State X=0	Next State x=1
A	B,0	D,0
B	A,0	B,0
C	D,1	A,0
D	D,1	C,0

Code No: A0601, A5701

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, March/April 2011

DIGITAL SYSTEM DESIGN

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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1.a) Draw the state diagram, state table and ASM chart for a D Flip-Flop.

b Discuss the different components of ASM chart. [12]

2.a) Implement the logic function 'F' using ROM

$F = \overline{ABC + ABC + ABC + ABC}$

b Explain how a sequential circuit can be designed using CPLD? [12]

3.a) Show that the three paths indicated in the circuit as shown in Fig. 1 cannot be sensitized individually but can be sensitized simultaneously.

b) Classify faults and give some examples to each class. [12]

4.a) Write a D Algorithm and compare it with other test pattern generation methods.

b) How signature analysis is used for testing bridging faults? [12]

5. Consider the machine whose transition table is given in table shown in Fig 2. Design a checking experiment for this machine. [12]

q \ x	a	b	c	d
A	A, 0	B, 1	A, 0	D, 1
B	C, 1	A, 0	B, 0	A, 0
C	D, 1	B, 1	A, 1	B, 0
D	B, 0	C, 1	A, 1	C, 1

Fig: 2

6.a) What is PLA folding? Why it is needed?

b) Implement the following three Boolean functions with a PLA.

$F_1(A, B, C) = \varepsilon(0,1,2,4)$

$F_2(A, B, C) = \varepsilon(0,5,6,7)$

$F_3(A, B, C) = \varepsilon(0,3,5,7)$ [12]

7. Explain how to test a PLA circuits? [12]

8.a) Draw & Explain the Basic model of sequential circuit.

b) Give a state assignment without critical races to each of the following asynchronous machine shown in figure 3. [12]

q \ x	I_0	I_1	I_2	I_3
A	(A)	C	(A)	B
B	A	(B)	A	(B)
C	(C)	(C)	E	D
D	C	B	(D)	(D)
E	(E)	F	(E)	D
F	E	(F)	A	B

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

UNIT -I:

MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:

Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:

CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV:

CMOS Operational Amplifiers:

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OPAmp.

UNIT -V:

Comparators:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

COURSE COVERAGE SUMMARY
CMOS ANALOG INTEGRATED CIRCUIT DESIGN

S.No	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR(S)	PUBLISHERS	EDITION
1	CMOS Analog Circuit Design	I-V	Philip E. Allen and Douglas R. Holberg	Oxford University Press	International Second Edition/Indian Edition, 2010
2	Analysis and Design of Analog Integrated Circuits-	I,II	Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer	3. Wiley India,	4. Fifth Edition, 2010.
3	Analog Integrated Circuit Design	II,III,IV	David A. Johns, Ken Martin	Wiley Student Edn	2013

SEPTEMBER-2009 PAPER–SUPPLEMENTARY

1.a] Why is emitter resistor RE replaced by a constant current bias circuit in differential amplifier stage of an op-AMP?
b] Design the dual input balanced output differential amplifier with the current mirror bias (shown below) according to the following specifications:
i) Supply voltage Vs= ±12V
ii) Maximum output voltage swing – 6Vpp.

2.a] Briefly explain the need for compensating networks in op-Amps.
b] Explain in detail about advanced current mirror compensating network.

3.a] What is a comparator? List the important characteristics of the comparator.
b] Explain different types of comparators with neat circuit diagrams.

4.a] Explain about CMOS sample and Hold circuit with neat waveforms.
b] Design a second order Butterworth low pass filter with a cutoff frequency of 500 Hz and a pass band gain of -2. Assume that a 5V ± power supply and a CMOS clock are used. [Using MF5].

5.a] Give the procedure of design of Biquard switched capacitor filter. [filter is a low pass filter].
b] Explain the operation of switched capacitor gain circuit.

6.a] What is difference between A/D and D/A converters? Give one application of each.
b] Draw and explain the Nyquist rate D/A converter using binary sealed converter.

7.a] Compare the performance of different types of D/A converters?
b] Define the resolution, settling time and conversion time of D/A converters.
c] Explain the operation of cycle flash type A/D converter with a neat circuit diagram.

8.a] Write the differences b/w continuous time and discrete time filters.
b] Explain in detail about digital decimation filter.

MARCH-2009-PAPER–(REGULAR)

1.a) Deduce the small signal model for an n-channel MOSFET taking into account the body effect.
b) Justify the choice of pmos loads.

2.a) Discuss the design aspects of CMOS source follower and derive an expression for the gain.
b) Consider a source follower which is biased by a current mirror. The dimensions of all the transistors are $100\,\mu m/1.6\,\mu m$, $\mu_n C_{ox} = 90\mu A/V^2$, $\mu_p C_{ox} = 30\mu A/V^2$ I_{bias}=100 μA, $\gamma_n = 0.5V^{1/2}$, $r_{ds-0} = 8000L(\mu m)/I_D(mA)$. What is the gain of the stage?

3.a) State the limitations of single stage amplifiers.
b) Explain in detail the design and operation of cascade current mirror. Identify the limitations and suggest remedies.

4.a) Deduce the necessary condition that ensures zero input-offset voltage for a 2 stage OP amp.
b) Discuss the trade offs involved in selecting the input stage as p-channel or n-channel with respect to a 2 stage OP amp.

5. Discuss in detail the compensation of OP amp that makes it completely independent of process and temperature variations.

6.a) Discuss in detail the design features of fully differential folded cascade op amp.
b) Give an account of charge injection errors in connection with comparators and suggest a method to minimize the same.

7.a) Explain the following in the context of data converters:
i) Resolution
ii) Offset and gain error
iii) Accuracy
iv) Differential non linearity error
v) Monotonicity
b) Explain briefly a 3 bit flash A/D converter. State the salient issues in designing flash A/D converters.

8.a) Show that the dynamic range can be increased by over sampling.
b) Discuss the stability and linearity issues associated with delta sigma converters.

MARCH-2008 PAPER-(REGULAR)

1.a) Explain large signal modelling of single stage BJT amplifier with neat sketches.
b) Explain common source amplifier with current mirror active load.

2.a) Explain the effect of negative feedback on the frequency response of OP-AMP.
b) Explain about cascode (or) CE-CB operational amplifier and obtain AC analysis of it.

3.a) Explain about charge injection error.
b) With a neat circuit diagram explain Bi-CMOS comparator.
c) Write the comparisons between Latched and Bi-CMOS comparators.

4.a) What is a switched capacitor filter? List important features of it. How does it differ from an analog filter?
b) Explain the operation of Bimos sample and Hold circuit with neat waveforms.

5.a) Explain the operation of switched capacitor circuit with neat waveforms.
b) Briefly explain correlated double sampling techniques.

6.a) What is Quantization Noise? Explain in detail.
b) Explain the operation at D/A converters using Hybrid converter.

7.a) What are the performance limitations of converters?
b) Compare different types of A/D converters.
c) Explain Successive Approximation A/D converter with a neat circuit diagram.

8.a) What is over sampling? Explain over sampling with and without noise sampling.
b) Explain in detail about Band pass over sampling converter.

FEBRUARY-2007 PAPER

1.a) Derive an expression for the –3dB frequency of a bipolar CE amplifier.

b) In a CMOS source follower circuit all transistors have $W/L = 100\mu m,/1.6\mu m$ $\mu_n C_{ox} = 90\mu A/V^2$, $\mu_p C_{ox} = 30\mu A/V^2$, $I_{bias} = 100\mu A$, $r_n = 0.5V^{1/2}$, $v_{ds\text{-}n}{}^{(\Omega)} = 8000L\ (\mu m)/ID(mA)$. Determine the gain of the stage.

2.a) Draw the circuit of CMOS current mirror and explain its working principle.
b) Explain why source/emitter follower circuits exhibits large amounts of overshoot and ringing.

3.a) What are the ways of improving slew rate of 2-stage CMOS opamp? And derive an expression for slew rate of CMOS opamp.
b) Explain about various OPAMP compensation techniques.

4.a) What is CMFB circuit? What are various methods of designing CMFB circuits? And compare them.
b) Explain the principle of continuous time CMFB circuit.

5.a) Briefly explain about various performance parameters of sample-and-hold circuit.
b) Draw the circuit of switched capacitor circuit and explain its principle.

6.a) Compare and contrast CMOS and BICMOS sample and hold circuits and their performance.
b) Define the terms as referred to converters:
i) offset and gain error
ii) INL error
iii) DNL error
iv) Sampling time uncertainty.

7.a) Prove that the sinusoidal signal has 1.76dB more power than a random signal which is uniformly distributed.
b) Explain the principle of operation of dual slope A/D converter.

8.a) What are the advantages of 1-bit D/A converters?
b) Derive the component values of 1st order continuous time filter.

SEPTEMBER-2008 PAPER–(SUPPLEMENTARY)

1.a) Derive an expression for gm of an N-channel MOS FET operating in linear and saturation regions.
b) Give the relative performance of CS, CG, CD amplifiers.

2.a) Discuss the design aspects of CMOS common source amplifier with diode connected load and derive an expression for the gain.
b) Consider a source follower which is biased by a current mirror. The dimensions of all the transistors are $100\mu m/1.6\mu m$, $\mu_n C_{ox} = 90\mu A/V^2$, $\mu_p C_{ox} = 30\mu A/V^2 I_{bias} = 100\mu A$, $\gamma_n = 0.5V^{1/2}$, $r_{ds-n} = 8000L(\mu m)/I_D(mA)$. What is the gain of the stage?

3.a) State the limitations of single stage amplifiers.
b) Explain in detail the design and operation of Wilson current mirror.

4.a) Deduce the necessary condition that ensures zero input-offset voltage for a 2 stage OP amp.
b) Discuss the trade offs involved in selecting the input stage as p-channel or n-channel with respect to a 2 stage OP amp.

5.) Discuss in detail the compensation of OP amp that makes it completely independent of process and temperature variations.

6.a) Give the significance of CMFB circuits.
b) Give an account of charge injection errors in connection with comparators and suggest a method to minimize the same.

7.a) Explain the following in the context of data converters:
i) Resolution
ii) Offset and gain error
iii) Accuracy
iv) Integral non linearity error
v) Missing codes
b) Explain briefly a 3 bit flash A/D converter. State the salient issues in designing Flash A/D converters.

8.a) Discuss in detail the nois shaped delta sigma modulator.
b) Write an account of band pass over sampling converters.

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

UNIT –I:MOS DESIGN

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II: Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design –Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III: Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edgetriggered flipflop.

UNIT –IV: Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –:Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design –Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits –A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

COURSE COVERAGE SUMMARY

CMOS DIGITAL IC DESIGN

S.No	TEXT BOOK TITLE	Chapters in Text Book	Units / Topics Covered	AUTHOR	PUBLISHERS	EDITION
1	Digital Integrated Circuit Design	1,2	UNIT-I MOS Design	Ken Martin	Oxford University press	2011
		2,3	UNIT-II Combinational MOS logic circuits			
		4,5	UNIT-III Sequential MOS logic Circuits			
2	CMOS Digital integrated circuits analysis and design	2,3	UNIT-IV Dynamic logic circuits	Sung-Mo Kang, Yusuf Leblebici	TMH	3rd .,2011
		4,5	UNIT-V Semiconductor memories			

M. Tech – I Semester Regular/Supplementary
Examinations, April, 2015
CMOS DIGITAL IC DESIGN
Time: 3 Hours
Max Marks: 60
Answer any FIVE questions
All questions carry EQUAL marks
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1(a) What are the criteria for voltage threshold for high level and low level in NMOS inverter characteristics? Explain.
(b) Determine the pull-up to pull-down ratio for an NMOS inverter.
2.(a) Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram.
(b) How the MOS inverters connected in cascade can drive large capacitive loads? Explain.
3.(a) Draw the CMOS full adder circuit and explain it s operation.
(b) Explain the propagation delay and power consumption issues of CMOS gate.
4.(a) Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table.
(b) Differentiate static and dynamic latches.
5(a) Explain the speed and power dissipation in dynamic CMOS logic.
(b) What are the various issues in CMOS dynamic logic design? Explain anyone with a neat sketch.
6.(a) What are the types of DRAM? Explain any one.
(b) Describe the leakage currents in DRAM cell.
7.(a) Explain the principle of NOR gate flash memory with a neat diagram.
(b) Compare the SRAM and DRAM.
8.Write short notes on
(a) Pseudo NMOS logic gate
(b) Dynamic pass transistor

II-SEMESTER

EMBEDDED REAL TIME OPERATING SYSTEMS

UNIT – I:
Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read,write), Process Control (fork, vfork, exit, wait, waitpid, exec.

UNIT - II:
Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS,Defining a Task asks States and Scheduling, Task Operations, Structure, Synchronization,
Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT - III:
Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT - IV:
Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V:
Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, Tiny OS, and Basic Concepts of Android OS.

TEXT BOOKS:
1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011
REFERENCE BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2007, TMH.
2. Advanced UNIX Programming, Richard Stevens
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh

EMBEDDED REAL TIME OPERATING SYSTEMS
COURSE COVERAGE SUMMARY

S.No	TEXT BOOK TITLE	Chapters in Text Book	Units / Topics Covered	PUBLISHERS	EDITION
1	**EMBEDDED REAL TIME OPERATING SYSTEM**	**1.ADVANCED UNIX PROGRAMMING**	**I**	**RICHARD STEVENS**	
2	**EMBEDDED REAL TIME OPERATING SYSTEM**	**2.REAL TIME SYSTEMS** **3.REAL TIME SYSTEMS** **4.VX WORKS PROGRAMM ERS GUIDE**	**II,IV** **III** **V**	**JANE W.S.LIU** **C.M.KRISHNA, KANG G.SHIN**	**PHI** **TMH**

Code No: D0604, D5703, D7703, D6803

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech II- Semester Regular Examinations September, 2010

EMBEDDED REAL TIME OPERATING SYSTEMS

(COMMON TO DIGITAL SYSTEMS & COMPUTER ELECTRONICS, VLSI SYSTEMS DESIGN/ VLSI/ VLSI DESIGN, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS)

Time: 3hours Max. Marks: 60 Answer any five questions

All questions carry equal marks

- - -

6. a) Write an algorithm for fork.
   How many types of system calls are there for messages? Write the algorithm for
   Msgsnd. [12]

2. a) What is a signal in UNIX? Explain classification of different groups of signals.
   b) Explain the necessary algorithm for attaching a shared memory. [12]

3. a) Differentiate between hard and soft real time systems.
   b) Discuss about the temporal parameters of real time workload. [12]

4. a) Explain the necessity of RTOS in an embedded system.
   b) Explain the weighted round robin and priority driven approaches of real time
   scheduling. [12]

5. a) What are the steps that almost eliminate a likely bug in program due to shared data problem?
   b) Discuss about priority Inversion problem and deadlock situation. [12]

6. What are the goals of operating system services? Discuss process management in
   detail. [12]

7. a) Discuss different ways of responding to a hardware resource call on interrupts.
   b) What are the salient features of µcos? [12]

8. a) What are the important functions present in kernelLib.h of Vxworks.
   b) Create a mutex semaphore using Vx works. [12]

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Code No: A3805

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Regular Examinations March/April 2010

EMBEDDED & REAL TIME SYSTEMS

(DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS)

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

- - -

1. Discuss about any four synthesis design Technologies.

2.a) What is meant by Hardware/Software co-simulation. Explain?
   b) Discuss about Priority inversion problem?
   c) Give the main features of Embedded Linux?

3.a) What are message queues? How to implement them?
   b) Explain the concept and implementation mechanism of pipes and signals?

4.a) Explain Scheduling algorithms of Embedded Task Scheduler?
   b) Discuss about semaphores and mutex?

5.a) What are concurrent processes? Explain how embedded software should deal concurrent processes?
   b) How to deal synchronization problems among processes? Explain with specific algorithms?

6.a) Discuss about Digital Signal Processor?
   b) Discuss basic features and frame format of Ethernet?

7. Write short notes on the following:
   i) RT-level Combinational logic.
   ii) Optimization of custom single purpose processors.
   iii) Goals of Embedded system.

8. Write short notes on:
   i) Features of Real time OS.
   ii) Blue tooth.
   iii) PSM-model.

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NR

Code No: B7001

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II - Semester Regular Examinations September, 2010
EMBEDDED AND REAL TIME SYSTEMS
(ELECTRONICS AND COMMUNICATIONS)

Time: 3hours **Max. Marks: 60**

Answer any five questions All questions carry equal marks

- - -

1. Explain the ARM processor, memory organization and instruction level parallelism.

2. a) Write a short notes on semaphore and queues.
   b) Explain the I2C bus and CAN bus.

3. Write a short note on
   a) Serial data communication
   b) Multiple interrupts.

4. Explain the embedded computing and embedded system design process.

5. What is meant by microprocessor and explain in detail the architecture of 8051 Microprocessor?

6. What are the various data transfer and logical instructions?

7. a) What is an interrupt?
   b) Explain the JUMP and CALL instructions.
   c) Arithmetic operation instructions.

8. a) Discuss about task and task states in Real-Time operating systems.
   b) Explain the memory management in RTOS environment.

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I- Semester Supplementary Examinations September, 2010
EMBEDDED REAL TIME OPERATING SYSTEMS
(COMMON TO DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS, ELECTRONICS & COMMUNICATION ENGINEERING)

Time: 3hours **Max. Marks: 60**

Answer any five questions All questions carry equal marks

- - -

1. Explain hard real time systems vs. software real time systems with suitable examples.

2. Write short notes on
   a) vfork b) wait c) fork d) exit.

3. Explain functional parameters with one suitable example.

4. a) What are the advantages and disadvantages of disabling interrupts during the running of a critical section of process?
   b) How does the card communicate with the host using the sockets?

5. Show then use of 15 points for the principles of RTOS based design by taking the example of digital camera.

6. Explain functions of device programmer.

7. a) Draw the state diagram of TCP stark generation.
   b) Why are the list of tasks and synchronization model required before using RTOS functions?

8. a) Why is Java popular for smartcard applications?
   b) Explain product design life cycle.

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Code No: C5502

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech I- Semester Supplementary Examinations September, 2010
EMBEDDED REAL TIME OPERATING SYSTEMS
(EMBEDDED SYSTEMS)

Time: 3hours Max. Marks: 60 Answer any five questions

All questions carry equal marks

- - -

1. Explain Inter process communication.

2. Write short notes on
   (a) Execution time
   (b) A periodic task

3. Explain all functional parameters with examples.

4.a) What are the parameters of a TCB of a task?

   b) What is meant by a pipe? How does a pipe differ from a queue?

5. Show the use of 15 points for the principles of RTOS-based design by taking the example of mobile phone device.

6.a) How do you set OS ENTER CRITICAL() and OS EXIT CRITICAL()? b) Explain the use of file descriptor for I/O devices and files.

7.a) Draw the state diagram of ACVM functions.

   b) Why is the I/O instructions platform dependant? Define throughput of an I/O system.

8.a) How does calling of an interrupt routine help in testing a design?

   b) Describe performance – acceleration methods.

--ooOoo--

CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT -I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, NoNideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing,biquad filters.

UNIT -II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities,Jitter in PLLs, Delay locked loops, applications
UNIT -III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:
Nyquist Rate A/D Converters:
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:
1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche,Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

CMOS MIXED SIGNAL CIRCUIT DESIGN

COURSE COVERAGE SUMMARY

	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR	PUBLISHERS	EDITION
1	Design of Analog CMOS Integrated Circuits	I,II	Behzad Razavi	TMH Edition	2002
2	CMOS Analog Circuit Design	II,IV	Philip E. Allen and Douglas R. Holberg	Oxford University Press,International Second Edition/Indian Edition	2010
3	Analog Integrated Circuit Design		David A. Johns,Ken Martin,	Wiley Student Edition,	2013

CMOS ANALOG & MIXED SIGNAL DESIGN

(DIGITAL SYSTEMS & COMPUTER ELECTRONICS)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

- - -1. a) Draw the circuit for a current source with CASCODE connection and explain about the significance of the circuit with necessary equations. Design a current source circuits with values 20 µA, 30 µA and 50 µA using MOSFET's.Draw the circuits and explain about the same. Given L = 5µ, V_{Gs} =1.2 V, V_{THP} = 0.91 V, KP = 18 µA / v. Assume standard values of any processdata required.

[12]

c) a) Derive the expression for time constant τ in the case of a current mirror circuit for a step input. Analyze the response of the circuit, giving explanation.

Design a current sink circuit using double cascade mirror circuit, given $V_{DD} = -V_{SS} =$ 2.5 V to sink a current of 15 µA, V_{Gs} = 1.5V, L = 5µ; W = 15µ.

$B_n = 60 \frac{\mu A}{v^2}$. λ = 0.06. [12]

b) a) Derive the expressions for R_{out} in the case of CMOS Wilson mirror circuit. Draw the circuit and explain the working.

CMOS regulated cascade current mirror circuit determine the values of R_{out},

given $V_{DD} = -V_{SS}$ = 2.5V, I_D = 10 µA, V_{Gs} = 1.3V, L = 5 µ. K_P = 60 µA / V^2,

W = 10 µ, V_{Gs} = 1.5V.

Draw the circuit for Resistor- MOSFET divider circuit and MOSFET only dividercircuit, giving explanation. Derive the expression for TC (V_{ref}) in the case of the above two circuits.

c) a) Derive the expression for bandwidth in the case of a PMOS source follower circuit with Active load.

i a) Draw the circuit for CMOS series- series circuit and its closed loop small-signal model and open loop model explaining its working.

iii) For the series shunt feedback amplifier derive the expressions for A_{OL}, β, R_i, R_o and A_{CL}. [12]

6. a) Draw the circuit for differential amplifier with current source load and explain its operation.

   b) Determine the values of +ve and –ve CMR and CMRR in the case of a differential amplifier, given for M6 with usual notation. W6 = 25 µ, L6 = 5 µ. ISS = 25 µA.

   Assume reasonable values of other data required if any. [12]

7. a) Draw the circuit for fully differential folded CASCODE OTA and explain its working.

b) Draw the schematic for CMOS analog multiplier Quad and deduce the expression

   for V_o. [12]

8. Write notes on any TWO

   a) Adaptive Biasing.
   b) DAC Architectures.
   c) ADC Architectures. [12]

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Code No: D5702, D7702, D6802

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II-Semester Regular Examinations September, 2010

CMOS ANALOG & MIXED SIGNAL DESIGN

Max.Marks:60

Answer any five questions All
questions carry equal marks - -

1a) Draw the circuit for regulated cascade current mirror and explain its working.

b) Design a wide-swing, low voltage current mirror circuit using CN20 process parameters, given $\Delta r = 0.37V$, $V_{THN} = 0.83$, $V_{Gs} = 1.2V$. Assume reasonable values of data required. [12]

2. a) Draw the circuit for three-MOSFET voltage divider and explain its operation.

b) Design a 5V voltage reference using three MOSFET voltage divider. Assume $V_{AD} = +5V$. $V_{SS} = 0V$. $I_D = 15\mu A$. $L_1 = L_2 = L_3 = 15\mu H$. [12]

3. a) Draw the circuit for Inode referenced self biasing circuit and explain its operation.

c) Design a 15µA current source using thermal voltage self biased reference. Assume reasonable values of design parameters. [12]

2 a) Draw the common source amplifier with current source load and explain its operations.

b) Using CN20 process parameters, determine the η for the NMOS source follower, assuming M2 of the circuit at 0V. $V_{SS} = -2.5v$. [12]

5. a) Draw the circuit for shunt-series feed back amplifier and explain its working.

Explain how the open loop parameters are estimated.

b) Calculate the gain of shunt – shunt amplifier assuming A = 600,000 V/A.

$R_i = 20\Omega$, $R_o = 20\ \Omega$. Assume reasonable values of data necessary. [12]

6. a) Draw the circuit of differential amplifier used to determine input common node range and explain about the same.

b) Draw the circuit for analog multiplier and explain its working. [12]

4. a) Draw the circuit for switched capacitor integrator and explain its working.

a Draw the circuit and explain how level shifting is done using p- channel source followers. [12]

c) Write notes on any **TWO**

Mixed signal layout issues.
ADC architectures.
c) CMOS comparator design. [12]

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LOW POWER VLSI DESIGN

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons,2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.

LOW POWER VLSI DESIGN

COURSE COVERAGE SUMMARY

S.NO	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR	PUBLISHERS	EDITION
1	Low-Voltage, Low-Power VLSI Subsystems	I,II,III,IV,V	Kiat-Seng Yeo, Kaushik Roy	TMH Professional Engineering.	
2	CMOS Digital Integrated Circuits Analysis and Design	IV,V	Sung-Mo Kang, Yusuf Leblebici,	TMH	2011.
3	Introduction to VLSI Systems A Logic, Circuit and System Perspective	I,II	Ming-BO Lin	CRC Press	2011

Code No: A7707 NR

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Regular Examinations March 2010

LOW POWER VLSI DESIGN

(COMMON TO EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS)

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

1.a) Discuss about the design limitations of power supply voltage, Threshold voltage, scaling and Inter connect wires on Low Power-Low voltage VLSI Design.

b) Explain about SOI technology and indicate how this technology helps in Low Power Design. [6+6]

2.a) Draw the cross sectional views of bipolar transistors suitable for integration with CMOS base line process.

b) Explain how isolation is provided in BI CMOS. [6+6]

3.a) What is the need for copper in integrated circuits? How does it help in Low Power-Low voltage VLSI Design? Explain about the process steps involved.

b) Give the Electrical Parameter values of Poly silicon-Emitter npn bipolar structure when operated at 5.0 and 3.3V. [6+6]

Explain about different types of advanced MOSFET models employed in Low-Power Design.

b) Explain about MEXTRAM Model of npn BJT. [6+6]

5.a) Draw the circuit for High-performance complimentary coupled BICMOS circuit and explain its working.

b) Draw the circuit for BI CMOS Buffer and explain the same. [6+6]

6. Draw the circuits for R-type, N-type (R + N) Type and Feed back type lugre circuits and explain the working of the same.

7.a) Explain about the evolution of latches and Flip Flops.

b) What are the major uses of latches and Flip Flops? Explain.

8. Write notes on any TWO:

a) UBIC 95 Model for MOSFETS
b) ESD-Free BI CMOS
c) Functionality Theme and synchronous Theme for latches and Flip-Flops.

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NR

Code No: B5506,B3806, B5703

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech II-Semester Regular Examinations September, 2010

LOW POWER VLSI DESIGN

(Common to Embedded Systems, DE&CS, VLSI System Design)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

- - -

1.a) What is meant by scaling in VLSI Design? What are the advantages of scaling? Explain.

b) Discuss about technology Node Variation, supply voltage, feature size and speed improvement variations in VLSI Design in the last twenty years.

2.a) Explain about process considerations of Emitter, Base and Collector in BI CMOS logic circuits.

b) Draw an nMOS Halo structure and explain the same.

3.a) Give the cross sectional view of a transistor fabricated using collector diffusion Isolation (CDI) process and explain the same.

b) With the help of neat sketches explain about side wall mask isolation process.

4. Give the typical values of various parameters of poly silicon – Emitter npn Bipolar structure when operated at 5.0V and 3.3V. Critically analyze the same.

5.a) Give the 0.2 μ m SOI BICMOS process flow with explanation.

b) With the help of necessary equations, explain about the properties of Fully depleted SOI MOSFETs. (FDSOI MOSFETS).

6.a) Using necessary equations, explain about Ebers-Moll model of BJT. Compare this with HICOM model.

b) Draw the BICMOS inverter circuits in Gated Diode (GD) and Emitter follower (EF) configurations and compare them.

7.a) Discuss about set-up, hold-time and full swing considerations of Low-Power Flip-Flops.

b) Derive the expressions for rise time and fall time in the case of a CMOS inverter, making necessary approximations.

8. Write notes on any **TWO**:

a) Performance measures of Low Power Flip-Flops.
b) Optimization theme for Flip-Flops.
c) ESD-free BICMOS.

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Code No: B5506

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II Semester Supplementary Examinations March 2010

LOW POWER VLSI DESIGN

(COMMON TO VLSI SYSTEM DESIGN, DE &CS, EMBEDDED SYSTEMS)

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

- - -

1.a) Explain about the Implications of

i) Power Supply Voltage
ii) Threshold Voltage and
iii) Scaling on Low voltage – Low power CMOS Design.

b) What are the advantages of Scaling in Low power VLSI Design? Explain. [6+6]

2.a) Draw the Cross sectional diagram of BiCMOS with npn Bipolar transistor using basic n-well CMOS process and explain the same.

b) Explain about Double Diffused Drain and Lightly doped Drain structures. [6+6]

3.a) With the help of neat sketches explain the process flow for polysilicon Emitter formation.

b) Give the typical values of Electrical Parameters of the Polysilicon – Emitter npn Bipolar structure when operated at 5.0V and 3.3V. [6+6]

4.a) Explain about MOSFET Level 1 Model and Level 2 Models.

b) Draw the equivalent circuit for npn Bipolar Ebers – Moll Model and explain the same. [6+6]

5.a) Draw the circuit for Common – Emitter BICMOS driver configuration and explain the characteristics.

b) Draw the circuit for Merged BICMOS NAND logic gate and explain its operation. [6+6]

6. Explain about the Quasi Complimentary BICMOS Digital Circuit and give the characteristics with typical values. [12]

7.a) Explain about the Performance Theme in Latches and Flip – Flops.

b) What are the Set – up and Hold Time Considerations in Flip – Flops? Explain. [6+6]

8.Write notes on any **TWO** [6+6]

a) ESD – free BICMOS Circuits
b) HICUM MOSFET Model
c) Lateral BJT on SOI

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DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE -III)

UNIT –I:

Introduction to Digital Signal Processing:

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences.Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems,Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:

Architectures for Programmable DSP Devices:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:

Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:

Analog Devices Family of DSP Devices:

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture,Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.

2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009

3. Embedded Signal Processing with the Micro Signal Architecture
Publisher: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.

2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.

4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI

5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D.,California Technical Publishing, ISBN 0-9660176-3-3, 1997

6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes ISBN 0750679123, 2005

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

COURSE COVERAGE SUMMARY

S.NO	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR	PUBLISHERS	EDITION
1	Digital Signal Processing	I,II,III,IV,V	Avtar Singh and S. Srinivasan,	Thomson Publications	2004.
2	A Practical Approach To Digital Signal Processing	IV,V	K padmanabhan, R. Vijayarajeswaran,Ananthi.	New Age International	2006 2009
3	Embedded Signal Processing with the Micro Signal Architecture	V	Woon-Seng Gan, Sen M. Kuo,	Wiley-IEEE Press, 2007	2007

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH II - SEMESTER EXAMINATIONS, APRIL/MAY 2012

DSP PROCESSORS AND ARCHITECTURES

(SYSTEMS AND SIGNAL PROCESSING)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

- - -

1.a) Explain how to design a bandpass filter using filter design and analysis tool with the following specifications:

Sampling frequency=300 KHz; Stop band frequency of 540-960 KHz; pass band frequency range of 600 – 900 KHz; attenuation on both sides of the pass band is 54db and pass band ripple of 1dB.

b) For the FIR filler described by the equation y(n) = 0.5*x(n) + 0.5*x(n-1). Find the unit sample response, frequency response, magnitude and phase response of the given system. Also find the group delay.

2.a) Compute the dynamic range and percentage resolution for a block floating point format with 4-bit exponent used in a 16-bit fixed point processor.

b) Compare the Microprocessor, Microcontroller and DSP processor with respect to all the features and explain how DSP processor is superior to them.

3.a) What is zero over head looping? How this feature is advantageous in DSP processor? Explain with an example.

b) Explain the following concepts of DSP processor
i) Interlocking
ii) Branching effects
iii) Interrupt effects

4.a) Explain which instruction is useful for repeating a set of instruction in a loop with an example program.

b) Explain the following on chip peripherals of the DSP processor.

i) Hardware timer
ii) Host port interface.
iii) Clock generator
iv) Serial I/O ports.

5.a) Explain the memory space organization of TMS320C54XX processor.

b) Explain how the signal spectrum is computed. Write a subroutine program that computes the spectrum using the FFT result.

6. Compare the following I/O interfacing methods

a) Programmed I/O with respect to DSP processor
b) Interrupt I/O
c) DMA.

7.a) Draw the block diagram of MCBSP of C54XX and also write a program that configures MCBSP to work with serial 20-bit input data and 20-bit output data.

b) Explain how PCM3002 provides 16-bit synchronous serial ADC and DAC.

8. Write short notes on any TWO

a) Decimation Filter
b) Implementation of PID Controller on TMS320C54XX
c) Q-notation and precautionary measures to be taken while using Q-notation in multiplication process

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech II Semester Supplementary Examinations March 2010

DSP PROCESSORS & ARCHITECTURE

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

1.a) Compute the FFT of the sequence $x(n) = \{1, 0, 0, 0, 0, 0, 0, 0\}$.

b) Explain and derive an expression for interpolation by a factor I, a process of sampling rate conversion both in time and frequency domain.

2. What are the basic operations in converting a digital signal into an analog signal? Explain.

3. Explain the basic architecture of DSP processor.

4. Explain the following terms with reference to DSP's.

   i) Interrupts.
   ii) Stacks.
   iii) Inter locking.
   iv) Interrupt effects.

5.a) Explain the data addressing modes of TMS320C54XX DSP's.

b) What are the on-chip pheripherals of DSP's TMS320C54XX?

6. Implement an algorithm for:

   i) Decimation filter
   ii) Adaptive filter.

7. Implement FFT algorithm for Butterfly computation.

8.a) Explain about Multi Channel buffered serial port in DSP's.

b) Explain DMA with reference to DSP's.

Code No: B5502, B6801, B5708

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech II Semester Examinations, October/November 2011

DSP PROCESSORS AND ARCHITECTURES

(COMMON TO EMBEDDED SYSTEMS, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEMS DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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1.a) In a DSP scheme show a continuous time signal, its sampled signal, sampled data signal Quantized digital signal & digital to analog converter output signal.

b) What is a system function? Explain how a LTI system is characterized. [12]

2. What is rounding error? Explain in context with ADC errors. Describe with an example ,DAC converter error due to the zero order. Differentiate between ADC and DAC errors in Computational accuracy in DSP. [12]

3.a) For a standard DSP FIR filter what are the basic features to investigate? Explain Organization of the On-Chip memory for DSProcesor.

b) Explain DSP Data addressing capabilities, with an example for each.

c) What are the special addressing modes in DSP? Give an example for each. [12]

4. Explain 3 stage pipelining and 5 stage pipelining, Justify your answer whether C54XX pipelining concept is employed. What is Perfect overlap in this situation seen in C54XX? What is pipeline hazard? With an example show reservation table for C54XX in pipelining. Explain Branching effects in pipelining. [12]

5. How will you configure a TMS320C5416 processor to have the following on chip memories? Specify the address range in: On chip ROM, for a program. How much RAM for data will be available in the specified configuration? [12]

6. Explain in detail PID controller in a continuous system. Explain the implementation of PID controller. [12]

7. Explain 4 point DFT computation with an example. [12]

8.a) Describe the memory interface block diagram of TMS320C5416.

b) Interface an 8Kx16 Program ROM to the C5416 in the address range 7FE000H-7FFFFFH.

c) Describe the I/O interface signals for READ-READ-WRITE sequence of operations. [12]

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CODE NO: B5708

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II SEMESTER EXAMINATIONS, OCTOBER/NOVEMBER-2012
DSP PROCESSOR AND ARCHITECTURES
(VLSI SYSTEM DESIGN)

Time: 3hrs **Max.Marks:60**

Answer any five questions
All questions carry equal marks

- - -

1.a) Explain about the Analysis and Design tools for DSP Systems listing all key features. Also explain how it supports multirate signal processing.

b) Explain any of the FIR Filter design methods in detail.

2.a) Given the FIR filter $y(n)=0.8x(n)+3x(n-1)+0.6x(n-2)$. Assuming the input range occupies ¼ of the full range, develop the DSP implementation equations in Q-15 format. What is the coefficient of quantization error?

b) Explain the following effects of finite fixed-point binary word length
i) Quantization Errors ii) ADC Coefficients iii) Truncation
iv) Rounding v) Data Overflow.

3.a) Define pipelining and pipeline depth Explain the concept of pipelining.

b) Draw a hardware schematic for MAC unit indicating the bit width of all signals. Also explain the advantages of MAC unit both in hardware and software perspective.

4.a) Explain the circular addressing mode of TMS 320C54XX processor with an example.

b) Explain the pipeline operation of the following sequence of TMS320C54XX instructions, if the initial value of AR3 is 80 and the values stored in the memory location 80, 81, 82 are 1, 2 and 3 respectively. Draw the pipeline operations.

5.a) Explain the implementation of an 8-point FFT on the TMS 320C54XX. Write an assembly language subroutine for bit–reversed order and twiddle factor calculation.

b) Write an assembly language program for the matrix multiplication of two matrices with size of 3X4 and 4X3 respectively.

6.a) Explain about the interrupts of TMS 320C54XX processor with table of interrupt locations and priorities.

b) Explain about interfacing a 2Kx16 block of memory to DSP processor.

7.a) Explain the method of Computing signal spectrum.

b) Explain about various external bus interfacing signals to a DSP Processor and explain their significance.

8.a) Explain how McBSP is useful for communicating with an external codec.

b) Explain how DMA controller makes the automatic data transfer between the McBSPs and the on-chip RAM.

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SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

UNIT –I:

Introduction to the System Approach:

System Architecture, Components of the system, Hardware & Software, Processor

UNIT –II:

Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

Simple Processor – memory interaction.

UNIT –III:

Memory Design for SOC:

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT -IV:

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2 nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1 st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L,2001, Kluwer Academic Publishers.

SYSTEM ON CHIP ARCHITECTURE
COURSE COVERAGE SUMMARY

S.NO	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR	PUBLISHERS	EDITION
1	Computer System Design System-on-Chip	I,II,III,IV,V	J. Flynn and Wayne Luk	Wiely India Pvt. Ltd.	
2	ARM System on Chip Architecture	IV	Steve Furber	Addison Wesley Professional.	2 nd Ed., 2000,
3	Design of System on a Chip: Devices and Components –	III,V	Ricardo Reis	Springer	1 st Ed., 2004,

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech II - Semester Regular Examinations September, 2010

SYSTEM ON CHIP ARCHITECTURE

(Common to Embedded Systems, Digital Systems & Computer Electronics, VLSI System Design /VLSI / VLSI Design, Embedded Systems & VLSI Design, VLSI & Embedded Systems)

Time: 3hours Max. Marks: 60 Answer any five questions

All questions carry equal marks

iii) a. Explain a Manchester processor design for MUn where n = 0 simple processor.

What is a Pipeline Hazard? Give an example. Explain Pipelined branch behavior.

iv) What is the difference between 3 & 5 stage pipelining? Which features of ARM Architecture are not shared by most other RISC's?

v) a. Write an ARM assembly language to Print "Hello world" on the display before terminating.
Explain Stack addressing and Block copy addressing in ARM.

a. Explain how ARM handles memory faults detected during Instruction fetch and Data transfer separately.

Explain the control flow and Conditional execution instruction in ARM. Give example.

a.Explain Normal, Efficient and Packed Structure memory allocation.

Show how the following data is organized in memory. Struct SI {char c; int x;}; struct
S2 {

Char
c2[5];
SI si[2];

}

Example;

6. a.Explain ARM's Cache organization.

   b. Explain Direct Mapping.

7. a.Explain Basic ARM Memory Interface system.

   b. Explain Advanced Micro controller Bus Architecture.

8. Write short notes on any **TWO** of the following.

   a. Synchronization, Mutual exclusion and context switching.
   b. Cache organization Options.
   c. Thumb Properties.

GRID AND CLOUD COMPUTING
(Elective-IV)

UNIT-I

System models for advanced computing –clusters of cooperative computing, grid computing and cloud computing; software systems for advanced computing-service oriented software and parallel and distributed programming models with introductory details, Features of grid and cloud platform.

UNIT-II

Cloud Computing services models and features in Saas, Paas and Iaas.
Service oriented architecture and web services; Features of cloud computing architectures and simple case studies.

UNIT-III

Virtualization- Characteristic features, Taxonomy Hypervisor, Virtualization and Cloud Computing, Pros and Cons of Cloud Computing, Technology Examples/Case Studies.

UNIT-IV

Cloud programming Environmental- Map Reduce Hadoop Library from Apache, Open Source Cloud Software Systems –Eucalyptus.

UNIT-V

Grid Architecture and Service modeling, Grid resource management, Grid Application trends.

TEXT BOOKS:

1. Distributed and Cloud Computing, Kaittwang Geoffrey C.Fox and Jack J Dongrra, Elsevier India 2012.
2. Mastering Cloud Computing- Raj Kumar Buyya, Christian Vecchiola and S.Tanurai Selvi, TMH, 2012.

REFERENCE BOOKS:

1. Cloud Computing, John W. Ritting House and James F Ramsome, CRC Press, 2012.
2. Enterprise Cloud Computing, Gautam Shroff, Cambridge University Press, 2012.

GRID AND CLOUD COMPUTING

COURSE COVERAGE SUMMARY

S.No	TEXT BOOK TITLE	Units / Topics Covered	AUTHOR(S)	PUBLISHERS	EDITION
1	Distributed and Cloud Computing,	I-V	Geoffrey C.Fox and Jack J Dongrra, .	Elsevier India	2012
2	Mastering Cloud Computing	I-V	1. Raj Kumar Buyya, Christian Vecchiola and S.Tanurai Selvi,	TMH	2012